

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Apparatus for processing data, comprising:

a circuit used in processing data, said circuit having one or more nodes for storing one or more data values that together define a state of said circuit;

a memory for storing data;

a multi-bit wide system bus, coupled to said circuit and said memory, for transferring multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory; and

a state saving controller, coupled to said circuit and said system bus, configured in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words[[-.]],

wherein said one or more nodes are each coupled to a respective scan chain cell within said circuit, said state saving controller being configured, in response to said state saving trigger, to store said data values within respective scan chain cells and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words, and

a plurality of scan chains, each containing a plurality of scan chain cells, said plurality of scan chains configured to operate in parallel to provide respective bits that together form a state saving multi-bit data word when said plurality of scan chains are serially read.

2. (Original) Apparatus as claimed in claim 1, wherein said circuit is a processor core.

3. Canceled.

4. Canceled.

5. (Currently Amended) Apparatus as claimed in claim 1, wherein said scan chain cells are also ~~operable~~ configured to perform test functions upon said circuit.

6. (Original) Apparatus as claimed in claim 1, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

7. (Currently Amended) Apparatus as claimed in claim 6, wherein said further memory is coupled to a built-in self-test controller operable to perform self-test operations upon said further memory and said state saving controller ~~is uses~~ configured to use said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

8. (Original) Apparatus as claimed in claim 1, wherein said memory transfers are burst mode memory transfers.

9. (Original) Apparatus as claimed in claim 1, wherein said state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

10. (Original) Apparatus as claimed in claim 1, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

11. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises execution of a state saving program instruction.

12. (Original) Apparatus as claimed in claim 1, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.

13. (Currently Amended) A method of saving state within an apparatus for data processing having:

a circuit used in processing data, said circuit having one or more nodes ~~operable to store~~  
for storing one or more data values that together define a state of said circuit;

a memory ~~operable to store~~ for storing data; and

a system bus coupled to said circuit and said memory ~~and operable to transfer for~~  
transferring multi-bit data words between said circuit and said memory in response to memory  
transfer requests issued upon said system bus during normal processing operation of said circuit  
and said memory; and

a plurality of scan chains each containing a plurality of scan chain cells,

said method comprising:

in response to a state saving trigger, using a state saving controller coupled to said circuit  
and said system bus to read said data values defining a state of said circuit from said one or more  
nodes and to generate a sequence of memory write requests on said system bus that write one or  
more state saving multi-bit data words representing said data values into said memory such that  
said state of said circuit is restorable using said one or more state saving multi-bit data  
words[.].

wherein said one or more nodes are each coupled to a respective scan chain cell within  
said circuit, said state saving controller, in response to said state saving trigger, storing said data  
values within respective scan chain cells and serially reading said data values from said scan  
chain cells to form said one or more state saving multi-bit data words, and

said plurality of scan chains operating in parallel to provide respective bits that together  
form a state saving multi-bit data word as said plurality of scan chains are serially read.

14. (Original) A method as claimed in claim 13, wherein said circuit is a processor  
core.

15. Canceled.

16. Canceled.

17. (Currently Amended) A method as claimed in claim ~~15~~13, wherein said scan chain cells ~~are also operable to perform~~ test functions upon said circuit.

18. (Original) A method as claimed in claim 13, wherein said circuit is a further memory and said data values are bits of data words stored in said further memory.

19. (Currently Amended) A method as claimed in claim 18, wherein said further memory is coupled to a built-in self-test controller ~~operable to perform~~ that performs self-test operations upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words.

20. (Original) A method as claimed in claim 13, wherein said memory transfers are burst mode memory transfers.

21. (Currently Amended) A method as claimed in claim 13, wherein said state saving controller, ~~is operable in response to a state restoring trigger, to generate~~ generates a sequence of memory read requests on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and ~~write~~ writes said data values represented by

said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit.

22. (Original) A method as claimed in claim 13, wherein said multi-bit state saving data words are stored in a user specified region of said memory.

23. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises execution of a state saving program instruction.

24. (Original) A method as claimed in claim 13, wherein said state saving trigger comprises initiation of a diagnostic test upon said circuit.